CLAIMS

WHAT IS CLAIMED IS:

1. A television receiving system comprising:

a plurality of television receiver mechanisms for receiving a plurality of separate television program signals;

a multiplexer mechanism coupled to the television receiver mechanisms for multiplexing the received program signals into a single combined signal stream;

a security mechanism responsive to the single combined signal stream for controlling access thereto;

a demultiplexer mechanism coupled to the security mechanism for receiving an access-allowed combined signal stream and demultiplexing same for producing separate television program signals corresponding to the separate program signals received by the receiver mechanisms;

and circuitry responsive to at least one of the demultiplexed separate program signals for supplying image signals to a television display mechanism for enabling same to produce television images.

2. In a television system, the combination comprising:

a multiplexer mechanism responsive to a plurality of separate television program signals for multiplexing the separate program signals into a single combined signal stream;

a security mechanism responsive to the single combined signal stream for controlling access thereto;

and a demultiplexer mechanism coupled to the security mechanism for receiving an access-allowed combined signal stream and demultiplexing same for producing separate television program signals corresponding to the separate television program signals received by the multiplexer mechanism.

3. The combination of Claim 2 wherein:

the multiplexer mechanism includes a plurality of input FIFO storage mechanisms for individually receiving different ones of the separate program signals and FIFO readout circuitry coupled to the outputs of the input FIFO storage mechanisms for producing a single combined signal stream ;

and the demultiplexer mechanism includes a plurality of output FIFO storage mechanisms and FIFO read-in circuitry coupled to the output of the security mechanism for transferring signal portions for the different program signals to their respective ones of the output FIFO storage mechanisms.

4. A digital television receiving system comprising:

a plurality of digital television receiver mechanisms for receiving a plurality of separate digital television program signal transport streams;

a multiplexer mechanism coupled to the digital television receiver mechanisms for multiplexing the received program signal transport streams into a single combined signal transport stream;

a security mechanism responsive to the single combined signal transport stream for controlling access thereto;

a demultiplexer mechanism coupled to the security mechanism for receiving an access-allowed combined signal transport stream and demultiplexing same for producing separate digital television program signal transport streams corresponding to the separate program signal transport streams received by the receiver mechanisms;

and circuitry responsive to at least one of the demultiplexed separate digital television program signal transport streams for supplying image signals to a television display mechanism for enabling same to produce television images.

5. In a digital television system, the combination comprising:

a multiplexer mechanism responsive to a plurality of separate digital television program signal transport streams for multiplexing the separate program signal transport

streams into a single combined signal transport stream;

a security mechanism responsive to the single combined signal transport stream for controlling access thereto;

and a demultiplexer mechanism coupled to the security mechanism for receiving an access-allowed combined signal transport stream and demultiplexing same for producing separate digital television program signal transport streams corresponding to the separate program signal transport streams received by the multiplexer mechanism .

6. The combination of Claim 5 wherein:

the multiplexer mechanism includes a plurality of input FIFO storage mechanisms for individually receiving different ones of the separate program signal transport streams and FIFO readout circuitry coupled to the outputs of the input FIFO storage mechanisms for producing a single combined signal transport stream ;

and the demultiplexer mechanism includes a plurality of output FIFO storage mechanisms and FIFO read-in circuitry coupled to the output of the security mechanism for transferring signal portions for the different program signal transport streams to their respective ones of the output FIFO storage mechanisms.

7. A signal transport stream multiplexing mechanism comprising:

a first FIFO storage mechanism for receiving signal packets in a first signal transport stream;

a second FIFO storage mechanism for receiving signal packets in a second signal transport stream;

and FIFO readout circuitry coupled to the outputs of the first and second FIFO storage mechanisms for reading signal packets from the first and second FIFO storage mechanisms in an interleaved manner for producing a combined signal transport stream.

8. A multiplexing mechanism in accordance with Claim 7 wherein the FIFO readout circuitry includes control circuitry for enabling each signal packet to be read out

only after the packet is fully resident in its FIFO storage mechanism .

9. A multiplexing mechanism in accordance with Claim 7 wherein the FIFO readout circuitry includes control circuitry for causing the next packet to be read from a different one of the FIFO storage mechanisms when such different one of the FIFO storage mechanisms has a packet ready for reading.

10. A multiplexing mechanism in accordance with Claim 7 wherein the FIFO readout circuitry includes control circuitry for switching to a different FIFO storage mechanism after each packet is read out, except that a second packet may be read from the same FIFO storage mechanism if it has a packet ready and the other FIFO storage mechanisms do not have a packet ready.

11. A multiplexing mechanism in accordance with Claim 7 and including a packet marker mechanism for receiving the packets in one of the signal transport streams and changing the coding of the sync byte in each such packet to a unique identifier value before it is supplied to its FIFO storage mechanism.

12. A multiplexing mechanism in accordance with Claim 11 wherein the packet marker mechanism comprises:

detector circuitry for detecting the occurrence of a sync byte and producing a control signal;

and exclusive OR circuitry responsive to the control signal for changing the coding of the sync byte to the unique identifier value.

13. A multiplexing mechanism in accordance with Claim 7 and including:

a first packet marker mechanism for receiving the packets in the first signal transport stream and changing the coding of the sync byte in each such packet to a first unique identifier value before it is supplied to the first FIFO storage mechanism ;

and a second packet marker mechanism for receiving the packets in the second

signal transport stream and changing the coding of the sync byte in each such packet to a second unique identifier value before it is supplied to the second FIFO storage mechanism.

14. A multiplexing mechanism in accordance with Claim 13 wherein each of the first and second packet marker mechanisms comprises:

detector circuitry for detecting the occurrence of a sync byte and producing a control signal;

and exclusive OR circuitry responsive to the control signal for changing the coding of the sync byte to the unique identifier value.

15. A transport stream demultiplexing mechanism comprising:

a first FIFO storage mechanism for supplying signal packets for a first program to a utilization mechanism;

a second FIFO storage mechanism for supplying signal packets for a second program to a utilization mechanism;

and FIFO read-in circuitry for separating signal packets for different programs from a combined program transport stream and transferring packets for a first program to the first FIFO storage mechanism and packets for a second program to the second FIFO storage mechanism.

16. A demultiplexing mechanism in accordance with Claim 15 and including control circuitry for enabling signal packets to be transferred from the FIFO storage mechanisms to the utilization mechanisms only after the packet is fully resident in its FIFO storage mechanism.

17. A demultiplexing mechanism in accordance with Claim 15 and including a packet marker mechanism for restoring the coding of the packet sync bytes for one at least of the programs to a normal sync code value before they are transferred to their

FIFO storage mechanism.

18. A demultiplexing mechanism in accordance with Claim 17 wherein the packet marker mechanism comprises:

detector circuitry for detecting the occurrence of a sync byte and producing a control signal;

and exclusive OR circuitry responsive to the control signal for restoring the coding of the sync byte to a normal sync code value.

19. A demultiplexing mechanism in accordance with Claim 15 and including packet marker mechanisms for restoring the coding of the packet sync bytes for both programs to a normal sync code value before they are transferred to their respective FIFO storage mechanisms.

20. A demultiplexing mechanism in accordance with Claim 19 wherein each packet marker mechanism comprises:

detector circuitry for detecting the occurrence of a sync byte and producing a control signal;

and exclusive OR circuitry responsive to the control signal for restoring the coding of the sync byte to a normal sync code value.

21. A digital signal processing system comprising:

signal processing apparatus for processing packetized digital signals;

packet marker apparatus for receiving a plurality of packetized signal transport streams and changing the coding of the packet sync bytes in the different streams to different unique values;

a multiplexer mechanism for receiving the outputs of the packet marker apparatus and interleaving the packets from the different transport streams and supplying the interleaved packet stream to the signal processing apparatus for processing thereby;

and a demultiplexer mechanism for receiving the processed packets from the signal processing apparatus and separating the packets into separate transport streams in accordance with the unique code values in their sync bytes.